AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 - 18 (cancelled)

19. (previously presented) An integrated circuit (IC) comprising:

a plurality of circuit rows;

at least one low voltage island in at least one of said plurality of circuit rows, circuit elements in each said at least one low voltage island being powered by a low voltage (V_{ddl}) supply; and

at least one high voltage island in said at least one of said plurality of circuit rows, circuit elements in each said at least one high voltage island being powered by a high voltage (V_{ddh}) supply, V_{ddh} being a higher voltage than V_{ddl}; and,

at least one level converter comprising:

a first buffer receiving an input signal from said at least one low voltage island, said first buffer being connected between a virtual supply and a supply return;

a second buffer receiving an output of said first buffer and connected between V_{ddh} and said supply return; and

a supply select between V_{ddh} and said virtual supply, said supply select receiving an output from said second buffer and selectively passing V_{ddh} or a reduced supply voltage to said virtual supply responsive to said output from said second buffer.

20. (original) An IC as in claim 19, wherein said second buffer is an inverter.

21. (original) An IC as in claim 19, wherein said supply select is a supply switch in parallel with at least one diode, both connected between said first supply and said virtual supply.

22. (original) An IC converter as in claim 21, wherein said supply switch is a field effect transistor (FET) gated by said output of said second buffer and said at least one diode is a diode connected FET.

23. (original) An IC as in claim 22, wherein said supply switch FET is a P-type FET (PFET) and said at least one diode connected FET an N-type FET (NFET) diode.

24. (original) An IC as in claim 23, wherein said at least one diode connected NFET is a pair of series connected NFET diodes.

25. (original) An IC as in claim 23, wherein said second buffer is a CMOS inverter.

26. (original) An IC as in claim 25, wherein said first buffer is a CMOS inverter.

27. (original) An IC as in claim 25, wherein said first buffer is a logic gate.

28. (original) An IC as in claim 25, wherein said logic gate is a NAND gate receiving a plurality of V_{ddl} inputs.

29. (previously presented) An IC as in claim 25, wherein said CMOS inverter includes an NFET having a threshold higher than other NFETs in said level converter.

30. (previously presented) An IC as in claim 19, wherein said reduced supply voltage is below V_{ddl}.